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# High Performance and Low Cost Single Switch Current-fed Energy Recovery Circuits for AC Plasma Display Panels

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**ABSTRACT**

A high performance and low cost single switch current fed energy recovery circuit (ERC) for an alternating current (AC) plasma display panel (PDP) is proposed. Since it is composed of only one power switch compared with the conventional circuit consisting of four power switches and two large energy recovery capacitors, the ERC features a simpler structure and lower cost. Furthermore, since all power switches can be switched under soft switching operating conditions, the proposed circuit has desirable merits such as increased reliability and low switching loss. Specifically, there are no serious voltage notches across the PDP with the aid of gas discharge current compensation, which can greatly reduce the current stress of all inverter switches, and provide those switches with the turn on timing margin. To confirm the validity of proposed circuit, its operation and performance were verified on a prototype for 7-inch test PDP.

**Keywords:** Plasma display panel and energy recovery circuit

## 1. Introduction

In general, electronic display devices play an important role in information display for man-to-machine interface. With the rapid progress of the information industry, there has been a continuous increase in the demand for new electronic display devices with larger sizes, higher resolution, and higher information capacity. The recent interest in flat panel display devices has made PDP a promising candidate for the conventional Cathode Ray Tube (CRT) display, because the PDP is praised for its large screen size, wide viewing angle, thinness, and high contrast [1-10].

Fig. 1 shows the sectional view of a three-electrode type surface discharge AC PDP. As shown in this figure, the AC PDP is composed of addressing (A), sustaining (X), and scanning (Y) electrodes. The parallel display electrodes (i.e. X and Y electrodes) of 480 pairs, composed of transparent electrodes (ITO) and bus electrodes, form on the front glass substrate. A dielectric layer ($SiO_2$) and protective layer (MgO) are deposited on them. The addressing electrodes of 2556 lines (852X3 colors) orthogonal to display electrodes are formed on the rear glass substrate. Stripe barrier ribs are located between these addressing electrodes to separate each discharge cell. Three-color phosphors (i.e. red, green, and blue) are individually printed between barrier ribs [1-9].

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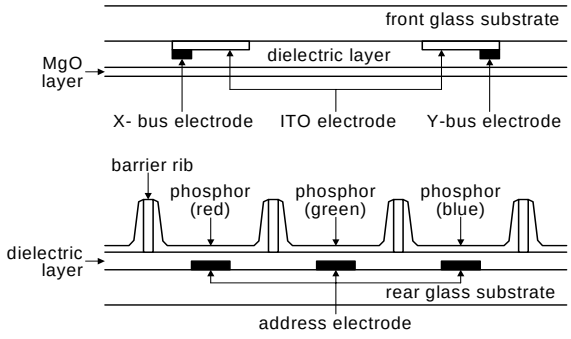


Fig. 1 Simplified sectional view of the three-electrode type surface discharge 42-inch AC PDP

The space between two-glass substrates is filled with a Ne and Xe gas mixture. Therefore, an AC high voltage will ionize the gas to create the plasma. Then, the ultraviolet (UV) rays from the plasma excite phosphors that emit the visible light.

Recently, a well-known Address Display Separation (ADS) driving method has been adopted to display images on the PDP by most PDP makers. In this method, the PDP operation is composed of three intervals: reset-, address-, and sustain-period. During the reset-period, all PDP cells are initialized and prepared to carry out address-operation by forming adequate wall charges on each electrode. During the address-period, selective write-discharges are ignited to form a required image by applying data and scan pulses to addressing and scanning electrodes, respectively. However, since the address-discharge itself emits insufficient visible light, AC high-voltage square-wave sustaining pulses generated by the sustain circuit are continuously applied between X and Y electrodes for the strong light emission of selective cells during the sustain-period [9, 10].

To generate these AC high-voltage sustaining pulses and process the resultant gas discharge current in the AC PDP, a well-known simple full bridge inverter (i.e., sustain circuit) can be adopted to convert a direct current (DC) voltage to a high frequency AC voltage. However, as mentioned above, the PDP is a capacitive load $C_p$. Therefore, when applying AC high voltage and high frequency square-wave pulses between X and Y electrodes, subsequent excessive surge charging and discharging currents will give rise to EMI noises and heating problems in all switching devices [1-9]. Specifically, this surge current could generate considerable energy loss (i.e., over 100W in the case of 42-inch SD-class PDPs) in the non-ideal resistance of circuits and PDPs during a charging or discharging interval.

To relieve these problems, several prior ERCs have been proposed. The circuits proposed in [2, 3] feature a very simple configuration. However, their fatal drawback is an overly large circulating current continuously flowing through each device. Therefore, in practical implementations, they require expensive power devices with larger current ratings. Moreover, their excessive circulating energy, subsequent conduction loss, and considerable heat generation degrade the overall system efficiency and performance. In addition, to implement the ADS driving method, several additional power switches must be employed to block the inductor leakage current during reset and address period, which results greater power loss and cost. The circuit proposed in [4] can be simply implemented with only one auxiliary power switch, two capacitors, and one inductor. However, since the large inductor current always circulates in the same manner of the circuit proposed in [3], its conduction loss and heat generation are still serious detriments. In addition, since the auxiliary switch handles the total circuit current including inductor and gas discharge currents, the burden on that switch is severe. Therefore, all above mentioned circuits are not suitable to the commercial scale product.

Meanwhile, due to its high efficiency and good circuit flexibility in coping with various driving methods, the circuit proposed by L. F. Weber et al., is most popular and usually adopted by most PDP makers such as Samsung, LG, Orion, FHP, and Matsushita [5]. Although this circuit can recover effectively most of the lost energy, it still has several undesirable drawbacks. First, since the two large auxiliary ERCs on both sides of the PDP are composed of four power switches, eight power diodes, two inductors, and two energy recovery capacitors as shown in Fig. 2, the cost of production is high and the system is complex and bulky. Secondly, energy-recovery capacitors are charged and discharged at a high frequency. As a result, the considerable heat generated by the equivalent series resistance (ESR) of energy recovery capacitors would shorten their lifetime. Therefore, several parallel-connected miler capacitors with a low ESR must be used instead of

an electrolytic capacitor, which also increases the cost of production. Furthermore, when charging and discharging the PDP, parasitic components such as a non-ideal resistance and diode forward voltage drop prevent the panel voltage from being fully charged to $V_s$ or discharged to 0V as shown in Fig. 4. All inverter switches might be turned on under hard switching operating conditions, resulting in an excessive surge current, serious power dissipation, EMI problems, and poor energy recovery efficiency. Therefore, this hard switching operation would cause the undesirable voltage oscillation across the PDP, serious wall charge loss, and reduced efficiency voltage applied to the PDP.

To overcome these drawbacks, a new high-performance and low cost current-fed energy recovery circuit for an AC plasma display panel (PDP) is proposed in this paper as shown in Fig. 5. Since the proposed circuit has only one power switch, two inductors, and eight diodes instead of the conventional large auxiliary circuit, it has significant advantages such as a simpler structure, fewer power devices, less mass, and lower cost. Furthermore, the current built in inductors $L_1$ and $L_2$ before inverting the panel voltage can fully charge and discharge the PDP regardless of parasitic components. This helps to achieve the zero voltage switching (ZVS) of all inverter switches, clear surge current, reduce EMI noise, and improve energy recovery capability. The gas-discharge current flowing through all inverter switches can be greatly reduced through the aid of gas discharge current compensation. Therefore, the clean panel voltage can ensure a more improved operational voltage margin, and more accumulated wall-charge. In addition, since the circulating current and subsequent conduction loss are very small besides the ZVS of all power switches, its overall system efficiency is very high and the burden on the cooling system is very light, which can be achieved in the fan-less system.

## 2. Review of prior circuit

In charging or discharging $C_p$, each equivalent circuit of the Weber circuit is formed as shown in Fig. 3, where $R_{esr}$ means the non-ideal resistance of circuits and $V_{on}$ forward voltage drops of diodes $D_{yu1}$, $D_{yl1}$, $D_{xu1}$, and $D_{xl1}$. From this figure, the panel voltage $v_{Cp}(t)$ during charging and discharging transients can be obtained as follows:

- In charging $C_p$:

$$v_{Cp}(t) = \left(\frac{V_S}{2} - V_{on}\right)\left\{1 - e^{-t/\tau}\left(\cos\omega t + \frac{1}{\omega\tau}\sin\omega t\right)\right\} \quad (1)$$

- In discharging $C_p$:

$$v_{Cp}(t) = \left(\frac{V_S}{2} + V_{on}\right) + \left(\frac{V_S}{2} - V_{on}\right)e^{-t/\tau}\left(\cos\omega t + \frac{1}{\omega\tau}\sin\omega t\right) \quad (2)$$

where $\tau$ is the time constant $2L_1/R_{esr}$, $\omega$ resonant angular frequency $\{1/\{L_1(C_p+2C_{oss})\}-1/\tau^2\}^{0.5}$, and $C_{oss}$ output capacitor of power switch

Based on equations (1) and (2), the voltage waveforms across PDP can be plotted as shown in Fig. 4. After a half cycle resonance between $L_1$ and $C_p$, the voltage across $C_p$ becomes $(V_s/2\text{-}V_{on})(1+e^{-\pi/(\omega\tau)})$ and $(V_s/2+V_{on})\text{-}(V_s/2\text{-}V_{on})$ $e^{-\pi/(\omega\tau)}$ in charging and discharging $C_p$, respectively. when M1 is turned on to sustain $C_p$ at $V_s$, the voltage difference as high as $V_s\text{-}(V_s/2\text{-}V_{on})(1+e^{-\pi/(\omega\tau)})$ between $v_{Cp}$ and input source $V_s$ causes a serious hard switching of M1, resulting in an excessive surge current. Similarly, when M3 is turned on to sustain $C_p$ at 0V, the voltage difference as high as $(V_s/2+V_{on})\text{-}(V_s/2\text{-}V_{on})e^{-\pi/(\omega\tau)}$ between $V_{Cp}$ and GND also causes serious hard switching of M3, resulting in an excessive surge current.

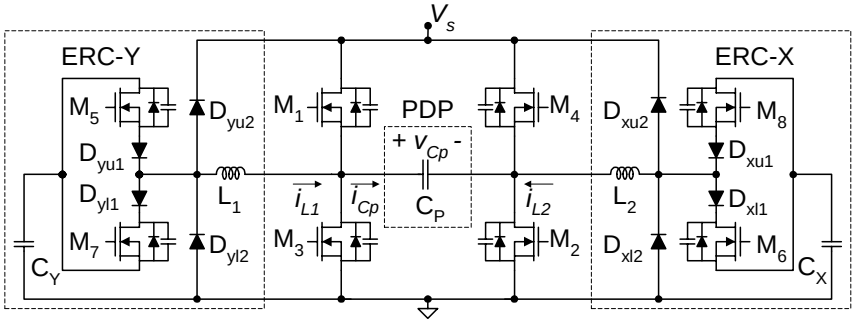


Fig. 2 Electrical equivalent circuit diagram of Weber circuit during sustain period

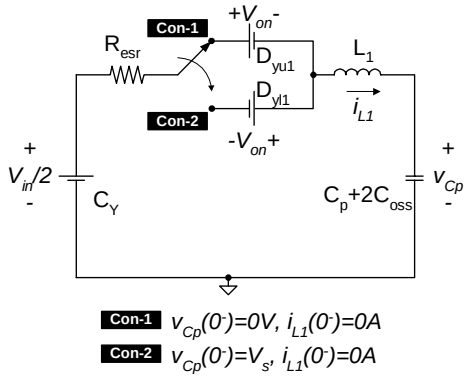


Fig. 3 Equivalent circuit in charging and discharging $C_p$

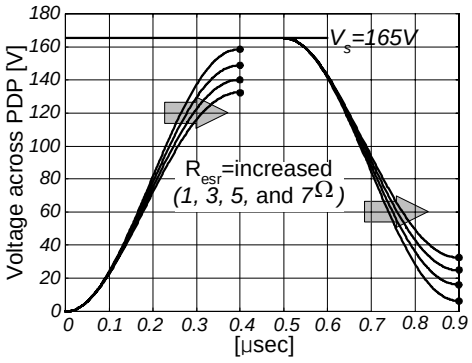


Fig. 4 Theoretical voltage waveform across PDP: $V_s$=165V, $V_{on}$=1.3V, $C_p$=1.6nF (7-inch PDP), power switch=2SK2995 ($C_{oss}$=1.9nF), rising time=0.4usec, $L_1$=$L_2$=2.95uH

These facts imply that the increase of parasitic resistance and diode forward voltage drop causes a serious hard switching operation, subsequent excessive surge current, serious power dissipation, EMI problems, and poor energy-recovery capability. To solve these problems, it is necessary to reduce the parasitic component by designing the circuit board optimally as well as choosing switching devices with the small on-resistance and low forward voltage drop. However, since it is impossible to get rid of parasitic components completely, the above-mentioned problems are inevitable. These problems would be more serious in a larger size PDP.

## 3. Proposed circuit

Figs. 5 and 6 show the proposed circuit and its key waveforms, respectively. One cycle period of the proposed circuit is divided into two half cycles, $t_0$~$t_4$ and $t_4$~$t_8$.

Because the operation principles of two half cycles are symmetric, only the first half cycle is explained. Before $t_0$, the voltage $v_{Cp}$ across $C_p$ is maintained to $V_s$ with $M_1$ and $M_2$ conducting as shown in Fig. 7 (a).

**Mode 1 ($t_0$-$t_1$):** When $M_5$ is turned on at $t_0$, mode 1 begins and the input voltage $V_s$ is applied to serially connected inductors $L_1$ and $L_2$ with $M_1$, $M_2$, $M_5$, $d_{y2}$, and $d_{x3}$ conducting as shown in Fig. 7 (b). Thus, $i_{L1}$ and $i_{L2}$ increase linearly with the slope of $0.5V_s/L$ as follows:

$$i_{L1}(t) = i_{L2}(t) = \frac{V_S}{2L}(t - t_0) \tag{3}$$

where it is assumed that $L_1$ and $L_2$ are all equal to L.

**Mode 2 ($t_1$-$t_2$):** When $M_1$ and $M_2$ are turned off at $t_1$, mode 2 begins. As shown in Fig. 7 (c), with the initial conditions of $i_{L1}(t_1)$=$i_{L2}(t_1)$=$I_{Lr}$=$0.5V_s(t_1$-$t_0)/L$ and $v_{Cp}(t_1)$=$V_s$, $i_{L1}$ and

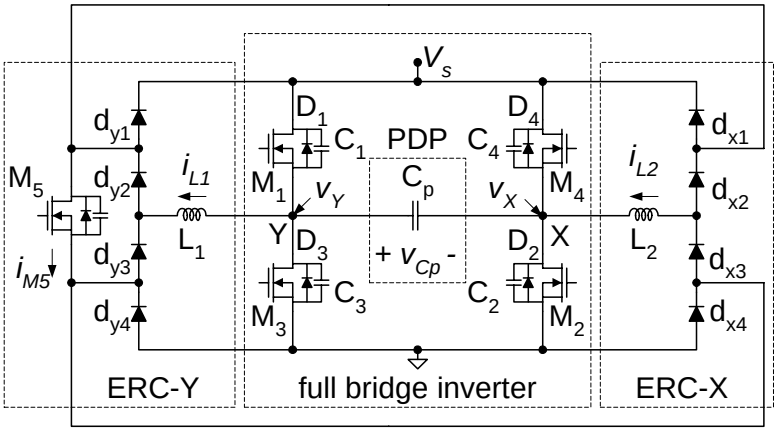


Fig. 5 Proposed Circuit

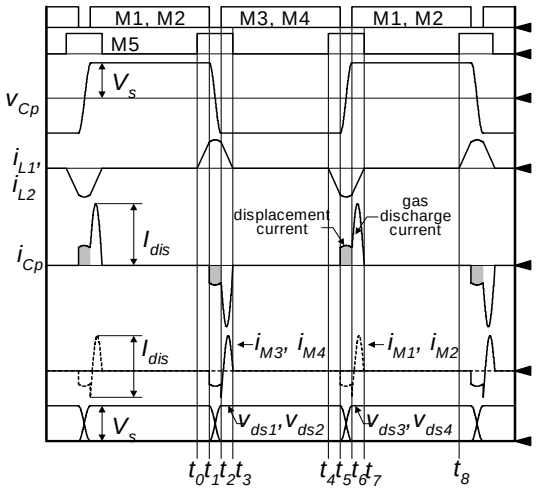


Fig. 6 Key operation waveforms of proposed circuit

$i_{L2}$ starts to charge the PDP, $C_1$, and $C_2$ and discharge $C_3$ and $C_4$ as follows:

$$i_{L1}(t) = i_{L2}(t) = I_{Lr}\cos\omega(t-t_1) + \frac{V_s}{Z}\sin\omega(t-t_1) \quad (4)$$

$$v_{Cp}(t) = V_S\cos\omega(t-t_1) - ZI_{Lr}\sin\omega(t-t_1) \quad (5)$$

where $C_1$, $C_2$, $C_3$, and $C_4$ are assumed to be equal to $C_{oss}$, $\omega = 1/\{2L(C_{oss}+C_p)\}^{0.5}$, and $Z=\{2L/(C_{oss}+C_p)\}^{0.5}$.

With this arrangement, the abrupt charging and discharging operations of $C_p$ are avoided and the voltage across $C_p$ is decreased toward $-V_s$.

**Mode 3 ($t_2$-$t_3$):** When $v_{Cp}$ is clamped at $-V_s$, $V_X$ gets to $V_s$, and $V_Y$ drops to 0V at $t_2$, mode 3 begins. Since the voltages $V_{ds3}$ and $V_{ds4}$ across $M_3$ and $M_4$ are 0V, $M_3$ and $M_4$ can be turned on with the ZVS as shown in Fig. 7 (d). Moreover, since inductor currents $i_{L1}$ and $i_{L2}$ compensate a large portion of the gas discharge current $I_{dis}$ during this period, the gas discharge current through $M_3$ and $M_4$ are considerably reduced as shown in Figs. 6 and 7 (d). During this mode, the inductor current begins to decrease linearly with the slope of $-0.5V_s/L$ as

$$i_{L1}(t) = i_{L2}(t) = I_{Lf} - \frac{V_S}{2L}(t-t_2) \quad (6)$$

where $I_{Lf}=i_{L1}(t_2)=i_{L2}(t_2)$.

**Mode 4 ($t_3$-$t_4$):** After the currents through $L_1$ and $L_2$ become 0A, M5 is turned off with zero current switching (ZCS) and thus, the turn off loss of M5 can be minimized. The panel capacitor voltage is still maintained at $-V_s$ with $M_3$ and $M_4$ conducting. This mode ends at $t_4$ when $M_5$ is turned on again.

The circuit operation of $t_4$-$t_8$ is similar to that of $t_0$-$t_4$. Subsequently, the operation from $t_0$ to $t_4$ is repeated.

## 4. Features of the proposed converter

### 4.1 Gas discharge current compensation

Fig. 8 shows the inductor and gas discharge currents of the proposed circuit during the charging transient stage.

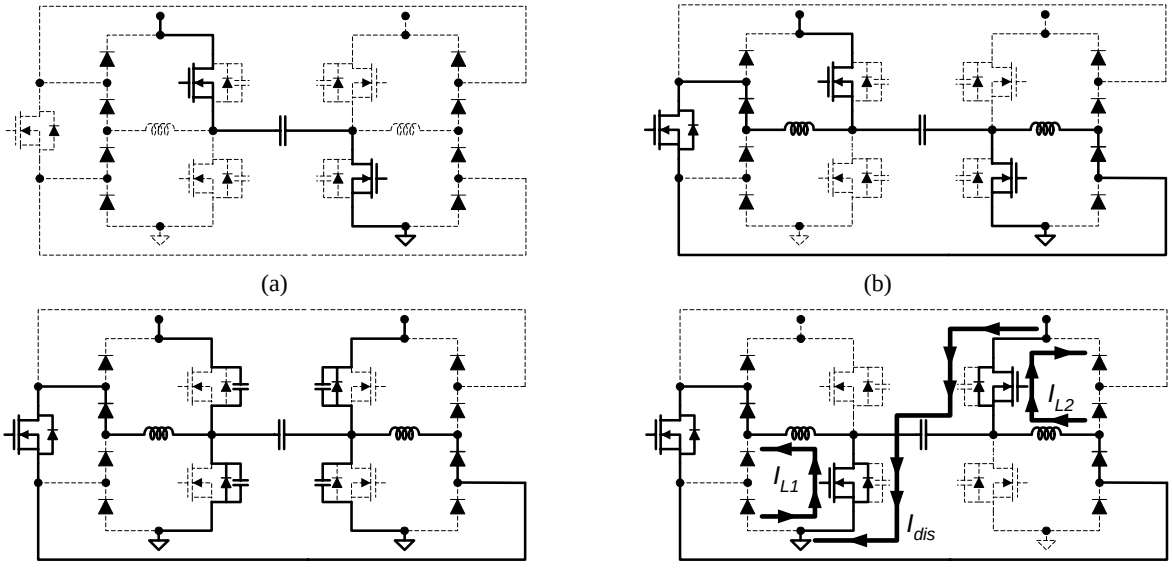


Fig. 7 Operation circuit diagram (a) before $t_0$ (b) at mode 1 (c) at mode 2 (d) at mode 3

As shown in this figure, Area-A is the current built in the inductors before inverting the panel voltage. Area-B is used to charge the panel capacitor and its average value is exactly the same as that of the conventional circuit. Area-D is utilized as the gas discharge current and thus, this part does not act as an additional conduction loss. Furthermore, this current (i.e. Area-D) can reduce the current stress, root mean square (RMS) value, and conduction losses of all inverter switches with its function of the gas discharge current compensation. Although Area-C is just fed back to the input power source and may somewhat increase the circulating energy without any energy recovery action, its value is not large enough to degrade the overall system efficiency and heating.

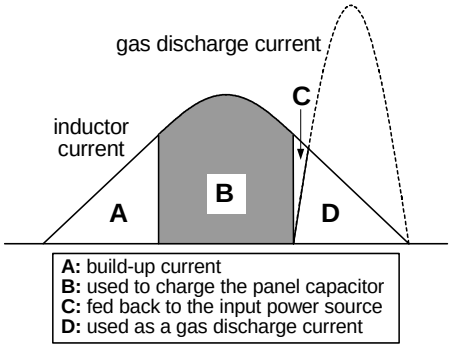


Fig. 8 inductor current and gas discharge current

### 4.2 Turn-on timing margin of main switch

The breakdown voltage of gas discharge is somewhat lower than the sustaining voltage $V_s$. Therefore, the gas discharge is ignited before the panel voltage arrives at $V_s$. However, if the transition time of panel voltage is fast enough (i.e. below an estimated 800nsec), the gas discharge can generally be ignited immediately after the voltage across PDP arrives at $V_s$.

If inverter switches M1~M4 are not turned on immediately after the voltage across the PDP arrives at the input voltage $V_s$, the voltage notch during cell discharge cannot be avoided in the conventional circuit as shown in Fig. 9 (a). Furthermore, since the exact time of the cell discharge varies according to the displayed image pattern, it is very difficult and may be impossible to specify the exact point of time ensuring no voltage notch. However, since the proposed circuit features the turn-on timing margin $T_m$ with the aid of inductor current as shown in Fig. 9 (b), no voltage drop can be ensured regardless of the displayed image pattern. Namely, the remaining inductor current can supply the gas discharge current until the main switch is turned on.

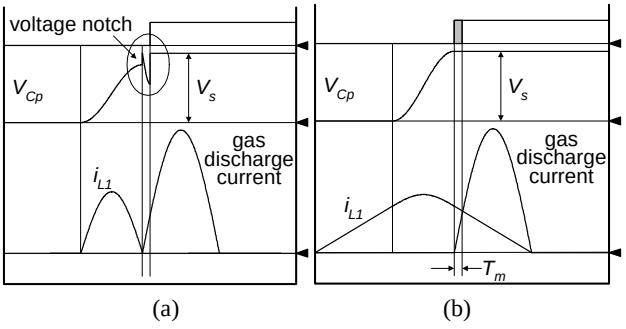


Fig. 9 Comparison of voltage drop across PDP
(a) Weber circuit (b) proposed circuit

### 4.3 Small number of devices and cost effectiveness

Table I shows the number of devices used to drive the 7-inch PDP. As shown in this table, the number of power switches used in the proposed circuit can be reduced by about 20%, which can also reduce the gate driving circuit including the expensive gate driver IC. Furthermore, while the Weber circuit has many expensive miler capacitors to recover the energy stored in PDPs, the proposed circuit has no additional capacitor. Therefore, it features a simpler structure, less mass, and lower cost of production.

Table 1 The number of devices used to drive 7-inch PDP

| Items | | Weber circuit | Proposed circuit |
|---|---|---|---|
| power switch | inverter | 2SK2995: 4(EA) | 2SK2995: 4(EA) |
| | auxiliary circuit | 2SK2995: 4(EA) | 2SK2995: 1(EA) |
| energy-recovery inductor: $L_1$, $L_2$ | | 2.95uH: 2(EA) | 54uH: 2(EA) |
| power diode | | SF20LC30: 8(EA) | SF20LC30: 8(EA) |
| gate driver IC | | IR2110: 4(EA) | IR2110[(1)]: 2(EA)<br>IR2118[(2)]: 1(EA) |
| energy recovery capacitor: $C_x$, $C_y$ | | miler 2.2uF/150V: 2 (EA) | 0(EA) |

(1) high and low side driver having one floating channel.
(2) single floating channel driver.

### 4.4 Soft switching operations of all power switches

As mentioned above, the current built in the inductor can accomplish the zero voltage turn on of all main power switches M1~M4. Moreover, since the auxiliary switch

M5 is turned off after the current through inductor becomes 0A, the zero current turn off of M5 can be obtained. Therefore, the switching loss and EMI problem can be solved.

### 4.5 Reduced current stress of all inverter switches

Since inductor currents compensate a large portion of the gas discharge current $I_{dis}(t)$ after inverting the panel voltage at $t_2$ of Fig. 6, the gas discharge current flowing through main switches M3 and M4 can be considerably reduced as

$$i_{ds3}(t) = i_{ds4}(t) = I_{dis}(t) - \left\{ I_{Lf} - \frac{V_S}{2L}(t - t_2) \right\} \quad (7)$$

Similarly, the gas discharge current through M1 and M2 can also be reduced as in M3 and M4.

## 5. Design considerations

### 5.1 Relationship among transition time Tt, build up time Tb, and inductor L

The brightness of a PDP increases with higher operating frequency or faster rising time. Thus, the transition time $t_1$-$t_2$=$t_5$-$t_6$ is required to be as short as possible considering the physical characteristics of PDP and system efficiency. Generally, the recommended transition time for the Xe-8% PDP is an estimated 800nsec. If it is assumed that the transition time $t_1$-$t_2$=$t_5$-$t_6$ is defined as $T_t$ and the current build-up time $t_0$-$t_1$=$t_4$-$t_5$ as $T_b$, the design equation can be obtained from equation (5) as

$$-V_s = V_s \cos \omega T_t - Z \frac{V_s}{2L} T_b \sin \omega T_t \quad (8)$$

From equation (8), the relationship among $T_t$, $T_b$, and L can be expressed as

$$T_t = \sqrt{2L\left(C_p + C_{oss}\right)} \left[ \cos^{-1}\left( -1 \Big/ \sqrt{1 + \left(\omega T_b\right)^2} \right) - \tan^{-1}\left(\omega T_b\right) \right] \quad (9)$$

This equation says that the transition time $T_t$ decreases as the build up time $T_b$ or inductor L increases.

In a practical implementation, the exact values of L and $T_b$ are quite difficult to obtain because of unpredictable parasitic components. Moreover, the value of inherent panel capacitor $C_p$ changes according to the on-and-off states of pixels. Therefore, the optimal values of L and $T_b$ for the minimum power consumption and maximum luminous efficiency must be tuned with the method of trial and error through experimentation along the various image patterns.

### 5.2 Conduction loss analysis according Tb and L

To suggest a more practical design guideline for the circuit parameters of $T_b$ and L, the relationships between conduction loss and circuit parameters are investigated. A realistic and effective approach has been recommended in [8]. For the convenience of analysis, most conduction losses are assumed to be generated by switching devices. Additionally, if the complete energy recovery operation of the PDP is assumed to be ensured, the values of $T_b$ and L mainly affect the conduction losses of the circuit. Therefore, the switching losses of all switching devices are excluded in this analysis.

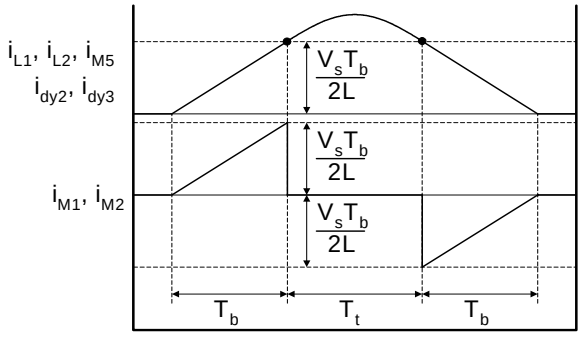


Fig. 10 Current waveforms through circuit devices during a half switching cycle

Based on mode analysis and Fig. 10, the conduction losses of inverter switches, auxiliary switches, and diodes averaged over a switching period $T_s$ can be obtained as follows:

• Total conduction loss $P_{cld}$ of diodes $d_{y2}$, $d_{y3}$, $d_{x2}$, and $d_{x3}$:

$$P_{cld} = \frac{1}{T_s} \left[ \begin{array}{l} 2\int_0^{T_b} \left( \frac{V_s}{2L} t \right) V_{on\_cld}\, dt \\ + \int_0^{T_t} \left( \frac{V_s T_b}{2L} \cos \omega t + \frac{V_s}{Z} \sin \omega t \right) V_{on\_cld}\, dt \end{array} \right] \times 4 \quad (10)$$

• Total conduction loss $P_{sw\_m}$ of inverter switches $M_1$, $M_2$, $M_3$, and $M_4$:

$$P_{sw\_m} = \frac{1}{T_s}\left[\int_0^{T_b}\left(\frac{V_s}{2L}t\right)^2 R_{ds}dt + \int_0^{T_b}\left(\frac{V_s}{2L}t\right)V_{on\_bd}dt\right]\times 4 \quad (11)$$

• Conduction loss $P_{sw\_aux}$ of auxiliary switch M5:

$$P_{sw\_aux} = \frac{2}{T_s}\left[\begin{array}{l} 2\int_0^{T_b}\left(\frac{V_s}{2L}t\right)^2 R_{ds}dt \\ +\int_0^{T_t}\left(\frac{V_sT_b}{2L}\cos\omega t + \frac{V_s}{Z}\sin\omega t\right)^2 R_{ds}dt \end{array}\right] \quad (12)$$

where $V_{on\_cld}$=forward voltage drop of $d_{y2}$ ($d_{y3}$, $d_{x2}$, and $d_{x3}$), $V_{on\_bd}$=forward voltage drop of anti-parallel diode $D_1$ ($D_2$, $D_3$, and $D_4$) of M1($M_2$, $M_3$ and $M_4$), and $R_{ds}$=on-resistances of $M_1$~$M_5$.

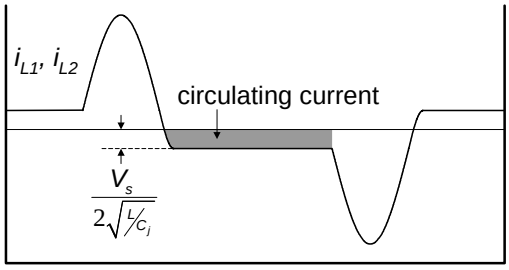


Fig. 11 Circulating inductor current

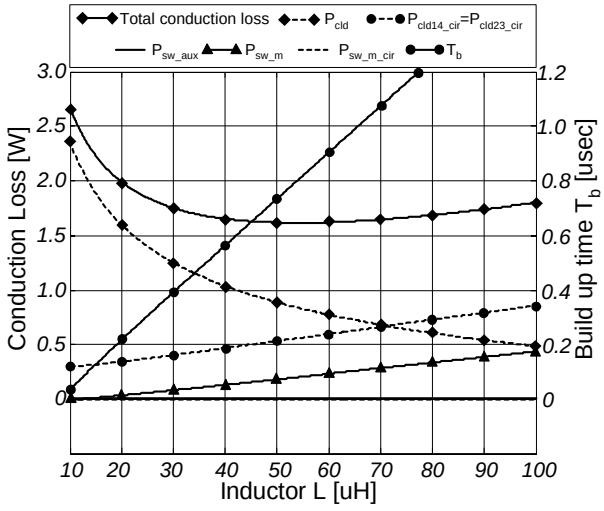


Fig. 12 Conduction losses and build up time according to various inductors: When $V_s$=165V, Switching period $T_s$=20usec, Transition time $T_t$=800nsec, PDP=7-inch ($C_p$=1.6nF), power switch=2SK2995 (Coss=1.9nF), diode= DF20LC30 (Cj=90pF)

Meanwhile, since the circulating current shown in Fig. 11 due to the junction capacitors $C_j$ of $d_{x1}$, $d_{x4}$, $d_{y1}$, and $d_{y4}$ cannot actually be ignored, the conduction loss caused by that current must be taken into account. The conduction losses of main switches and diodes caused by the circulating current averaged over a switching period $T_s$ can be expressed as follows:

• Total conduction loss $P_{cld14\_cir}$ of $d_{y1}$, $d_{y4}$, $d_{x1}$, and $d_{x4}$:

$$P_{cld14\_cir} = \frac{2}{T_s}\left[\int_0^{0.5T_s-2T_b-T_t}\frac{V_s}{2\sqrt{L/C_j}}V_{on\_cld}dt\right]\times 4 \quad (13)$$

• Total conduction loss $P_{cld23\_cir}$ of $d_{y2}$, $d_{y3}$, $d_{x2}$, and $d_{x3}$:

$$P_{cld23\_cir} = \frac{1}{T_s}\left[\int_0^{0.5T_s-2T_b-T_t}\frac{V_s}{\sqrt{L/C_j}}V_{on\_cld}dt\right]\times 4 \quad (14)$$

• Total conduction loss $P_{sw\_m\_cir}$ of $M_1$, $M_2$, $M_3$, and $M_4$:

$$P_{sw\_m\_cir} = \frac{1}{T_s}\left[\int_0^{0.5T_s-2T_b-T_t}\left(\frac{V_s}{\sqrt{L/C_j}}\right)^2 R_{ds}dt\right]\times 4 \quad (15)$$

Using equations (10)~(15), conduction losses and build up time satisfying the transition time $T_t$=800nsec according to various inductors can be calculated as shown in Fig. 12. As shown in this figure, the build up time $T_b$ increases to maintain the required transition time $T_t$ as the inductor increases. From these results, optimal circuit parameters L=54uH and $T_b$=800nsec can be obtained, at which the total conduction loss can be minimized..

## 6. Experimental results

The prototype of the proposed circuit is implemented with the specifications of $L_1$=$L_2$=54uH, $C_p$=1.6nF (7-inch Test PDP: manufactured by LG Electronics), $T_b$=800nsec, $M_1$, $M_2$, $M_3$, and $M_4$=2SK2995 ($C_{oss}$=1.9nF), gate driver IC=IR2110, switching frequency=50kHz, and Vs=165V. Fig. 13 shows the experimental results of the proposed circuit, when the white image is displayed. As can be seen in Fig. 13 (a), the current source built in the inductor completely charges the panel capacitor $C_p$ to $V_s$ or $-V_s$ without any hard switching and serious voltage notch across the PDP. Thus, the voltage waveform across PDP is very clean, which will attract more wall charge to deposit on the dielectric layer of the electrode. Furthermore, since

the current through inductor flows only when charging or discharging $C_p$, its circulating energy and conduction loss are very small compared with the circuits proposed in [2-4]. Fig. 13 (b) shows that $M_1$ and $M_3$ are turned on after $V_{ds1}$ and $V_{ds3}$ drop to 0V; that is, ZVS of $M_1$ and $M_3$ is achieved. $M_2$ and $M_4$ are also turned on with ZVS. Fig. 13 (c) shows that $M_5$ is turned off after $i_{ds5}$ becomes 0A; that is, the ZCS of $M_5$ is achieved.

In general, the overall system efficiency of the sustaining circuit for the PDP is defined as the energy recovery efficiency and expressed as

$$eff_{ER} = \left(\frac{I_{NER} - I_{ER}}{I_{NER}}\right) \times 100 = \left(1 - \frac{I_{ER}}{I_{NER}}\right) \times 100\ [\%] \qquad (16)$$

where $I_{NER}$ and $I_{ER}$ mean the averaged input current with and without the energy recovery circuit when no light is emitted, respectively. Namely, if it were not for non-ideal power losses generated by the parasitic resistance and other dissipative components, the energy recovery efficiency would be 100%, which is because the PDP has capacitive load characteristics.

Meanwhile, the luminous efficiency can be obtained from a following well-known equation:

$$\eta_{lumi} = \frac{3.14 \times DA \times (LW\text{-}LB)}{P_w - P_B} \qquad (17)$$

where DA=displayed area, LW=luminance at full white image [cd/m$^2$], LB=luminance at full black image [cd/m$^2$], $P_w$=input power at full white image, and $P_B$=input power at full black image.

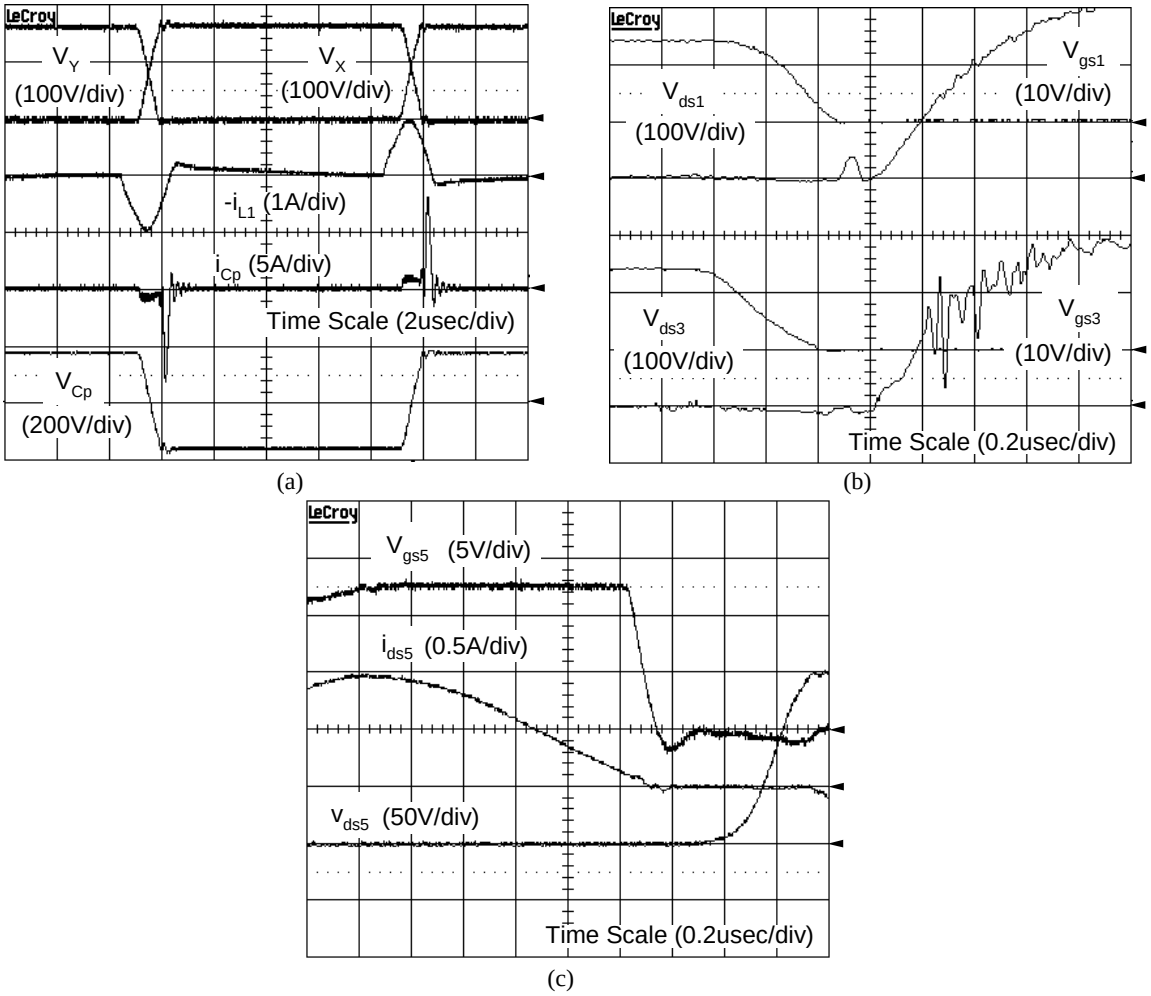


Fig. 13 Experimental waveforms of proposed circuit (In displaying white image) (a) Voltage waveforms across X, Y, and PDP and current waveform through $L_1$ and $C_p$ (b) ZVS turn on transients of $M_1$ and $M_3$, (c) ZCS turn off transients of $M_5$

Based on measured data and equations (16)~(17), the energy recovery and luminous efficiency can be calculated

as shown in Fig. 14. This figure shows that the proposed circuit has the higher energy recovery and luminous efficiencies than the Weber circuit which has the highest efficiency among hitherto developed ERCs.

This is due to the fact that the proposed circuit has several desirable advantages such as the completely charged and discharged PDP with no hard switching and voltage notch, less wall charge loss, soft switching operation of all power switches, and gas discharge current compensation of the inductor current. This result is especially meaningful in the sense that the proposed circuit using the small number of devices can achieve more improved efficiency and operational characteristics to the conventional ERC using a large number of devices.

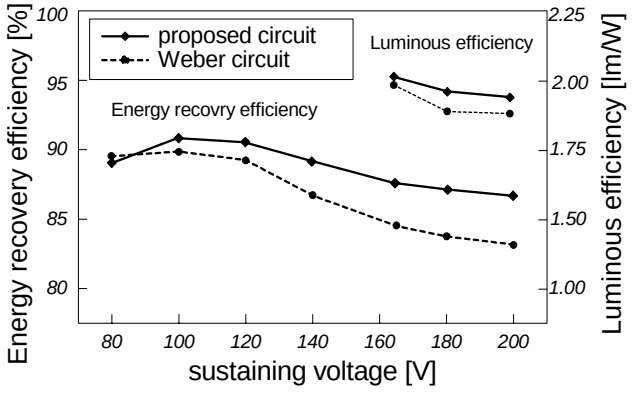


Fig. 14 Measured energy recovery efficiency and luminous efficiency

## 7. Conclusion

A new high-performance and low cost single switch current fed energy recovery circuit for an AC plasma display panel (PDP) was proposed to overcome the drawbacks of prior circuits and verified with a 7-inch test PDP. Experimental results show that the current source built in the inductor fully charges and discharges the PDP and all power switches are switched under soft switching operations. Moreover, the inductor current has a very narrow shape, which also means small conduction loss. Consequently, its energy recovery and luminous efficiencies are higher than the Weber circuit. Moreover, since it has only one auxiliary power switch, two small inductors, and eight diodes, it features a much simpler structure and lower cost. Since it compensates the large gas discharge current, it can solve the problem of undesirable voltage notch across the PDP, reduce the current stress of all inverter switches, and improve the turn-on timing margin. Additionally, the current source built in the inductor helps to reduce the transition time of panel polarity, which can increase the brightness. Therefore, the proposed circuit in this paper is expected to be well suited for high performance and low cost PDP TVs.

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